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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/890,894	07/16/97	CHAUVEL G	TI-25770

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 08/890,894	Applicant(s) Chauvel et al.
	Examiner Denise Tran	Group Art Unit 2752

☒ Responsive to communication(s) filed on *Sep 28, 1999*

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *three* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *6-19 and 34-39* is/are pending in the applicat

Of the above, claim(s) *none* is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *6-19 and 34-39* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☒ The proposed drawing correction, filed on *Sep 28, 1999* is ☒ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☒ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☒ received in Application No. (Series Code/Serial Number) *07/902,191* .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

DETAILED ACTION

1. The applicant's amendment filed 09/28/99 has been considered. Claims 1-5 and 20-33 have been canceled. Claims 6-19 and new added claims 34-39 are presented for examination.

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 36-39 are rejected under the judicially created doctrine of double patenting over claims 1-24 of U. S. Patent No. 6,000,026 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows: a main processor, a protocol processor, a synchronizing circuit, only one

common memory, and the protocol processor being suited to execute tasks to which the main processor is not suited.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

4. Claims 36-39 are rejected under the judicially created doctrine of double patenting over claim 1 of U. S. Patent No. 5,740,458 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows: a main processor, a protocol processor, a synchronizing circuit, only one common memory, and the protocol processor being suited to execute tasks to which the main processor is not suited.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the second processor for performing vector processing is a protocol processor (claim 16); and the second processor for performing vector processing, comprising: an incremental register connected to a program memory (claim 18). must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 19 and 35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 19, the phrases " said protocol processor" lack antecedent basis.

As per claim 35, the question mark at the end of the claim should be removed.

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claims 16 and 18 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In particular, the current application fails to teach the second processor for performing vector processing is a protocol processor (claim 16); and the second processor for performing vector processing, comprising: an incremental register connected to a program memory (claim 18).

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

11. Claims 6, 14-15 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Aoyama et al., U.S. Patent No. 4964035, (hereinafter Aoyama).

As per claim 6, Aoyama teaches the claimed invention, comprising: a first processor for performing scalar processing (e.g., fig.1, el. 600), comprising a core, a local memory, and a program memory (e.g., fig.1, els. 601 and 602; and col. 5, lines 47 et seq.); a second

processor for performing vector processing (e.g., fig. 1, el.500, vector processor), comprising a core, a local memory and a program memory (e.g., fig. 1, els. 501 and 502; and col. 8, lines 4 et seq.); a synchronizing circuit for coupling the core of the first processor to the core of the second processor (e.g., fig.1, els 810 or 800a, cols. 5-6); and a memory circuit for coupling the local memory of the first processor to local memory of the second processor (e.g., fig.1, el. 800).

As per claim 14, 15, and 17, Aoyama teaches the memory circuit coupling between the first and second processors being physically separate from the first and second processors (e.g., fig.1, el. 800); the memory circuit being DPRAM memory (e.g., col. 10); and the synchronizing circuit ensure that only one of the processors utilized the memory circuit at any one time (e.g., cols. 5-6).

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama as applied to claim 6 above, and further in view of Ngai et al., EP 0 157 306 A3, (hereinafter Ngai).

As per claim 7, Aoyama does not explicitly show the use of the second processor being a main processor. Ngai show the use of a main processor (e.g., abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Ngai into the Aoyama's system because it would provide for improving system performance by having a vector processor being a main processor to perform complex functions for the vector processor system.

14. Claims 8-13, 16, 18-19, and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al., U.S. Patent No. 4964035, (herein after Aoyama).

As per claim 8, Aoyama does not specifically show the scalar processor as a microprocessor. "Official Notice" is taken that both the concept and advantages of providing for the incorporation of a scalar processor into a microprocessor are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the incorporation of a processor into a microprocessor to Aoyama because it would provide for a reduction in chip space and signal lines between functional elements, leading to an increase in processing performance.

As per claim 9, Aoyama does not specifically show the second processor as a DSP. "Official Notice" is taken that both the concept and advantages of providing DSP to perform signal processing in the vector processing system are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a DSP into the vector processing system of Aoyama because it would provide for an increase in functionality in performing signal processing tasks.

As per claims 10-13 and 18, Aoyama does not specifically show the local memories as RAM; the program memory as a ROM; and the second processor comprising a ROM coupled to an incrementation register. "Official Notice" is taken that both the concept and advantages of providing a local memory as RAM; a program memory as ROM; and a ROM coupled to an incrementation register are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include RAMS; ROMs; and a ROM coupled to an incrementation register into the vector processing system of Aoyama because it would allow a storage location to be read and written in any order; a storage system to not loose data when power is removed from it.; and stepping through a program memory in the second memory.

As per claim 16, Aoyama does not specifically show the second processor being a protocol processor. "Official Notice" is taken that both the concept and advantages of providing a protocol processor are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a

protocol processor into the vector processing system of Aoyama because it would allow the system to encompass high level tasks.

As per claim 19, Aoyama shows the use of providing an instruction set to the first processor, comprising at least one field of execution conditions and classes of instructions: transfer operations between the memory and a register in the scalar processor, and monitoring scalar processing operations (e.g. cols. 1-2). Aoyama does not explicitly shows a transfer operations between a protocol processor and memory; and monitoring of all the operations modifying the value of an incrementation register in a protocol processor. "Official Notice" is taken that both the concept and advantages of providing integer instructions corresponding to ALU operations on integer numbers; providing a protocol processor in a vector-scalar processing system; and an incrementation register is well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include an integer instructions corresponding to ALU operations on integer numbers; providing a protocol processor with a register for transferring data; and an incrementation register in a protocol processor into Aoyama because it would allow the system to increase functionality by performing integer operations; and performing scalar processing high level tasks in the system.

As per claims 34-35, Aoyama teaches the vector processor and matrix computations; and the scalar processor (e.g., fig. 1., els 500 and 600 and cols. 1-2), but does not explicitly show the use of scalar processing encompassed a high level task which is the monitoring of an application or the management of functioning and tasks which are generally carry out by hard-

wired logic which are the protocol processing; and vector processing including signal processing tasks generally carrying out by a DSP and the use of array processor type. "Official Notice" is taken that both the concept and advantages of providing integer instructions corresponding to ALU operations on integer numbers; providing scalar processing encompassed a high level task which is the monitoring of an application or the management of functioning and tasks which are generally carry out by hard-wired logic which are the protocol processing; and vector processing including signal processing tasks generally carrying out by a DSP and the use of array processor type are well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor; and DSP and array processor into Aoyama because it would allow scalar processing to encompass high level tasks; and signal processing and matrix computations to be performed.

15. Claims 36-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama as applied to claim above, and further in view of Ngai et al., EP 0 157 306 A3, (hereinafter Ngai).

As per claims 36-39, Aoyama teaches the invention substantially as claimed, comprising: a first processor for performing scalar processing (e.g., fig.1, el. 600), comprising a core, a local memory, and a program memory (e.g., fig.1, els. 601 and 602; and col. 5, lines 47 et seq.),where the first processor being suited to execute tasks to which the main processor is not suited; a second processor for performing vector processing (e.g., fig.

1, el.500, vector processor), comprising a core, a local memory and a program memory (e.g., fig. 1, els. 501 and 502; and col. 8, lines 4 et seq.); a synchronizing circuit for coupling the core of the first processor to the core of the second processor (e.g., fig.1, els 810 or 800a, cols. 5-6); and one and only one common memory circuit for coupling the local memory of the first processor to local memory of the second processor (e.g., fig.1, el. 800). Aoyama does not explicitly show the use of the second processor being a main processor. Ngai show the use of a main processor (e.g., abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Ngai into the Aoyama's system because it would provide for improving system performance by having a main processor to perform complex operations for the vector processing system. Aoyama does not explicitly show the use of the first processor being a protocol processor. "Official Notice" is taken that both the concept and advantages of providing a protocol processor to a vector-scalar processing system are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a protocol processor to the system of Aoyama because it would allow the system to encompass scalar processing high level tasks.

16. Applicant's arguments with respect to claims 6-19 and 34-39 have been considered but are moot in view of the new ground(s) of rejection.

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (703) 305-9823. The examiner can normally be reached on Monday and Thursday from 8.30 to 6.00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Cabeca, can be reached on (703) 308-3116. The fax phone number for the organization where this application or proceeding is assigned is (703) 305-9731.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9600.

JOHN W. CABECA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2700

Denise Tran

01/06/00